IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
PRELIMINARY AMENDMENT	Atty. Docket No. (Opt.) **CVC1530-3**

Applicant: **Mehrdad M. Moslehi**	
Application Number **Unknown**	Filed **March 6, 2002**
For: **Ultra High-Speed Chip Semiconductor Integrated Circuit Interconnect Structure And Fabrication Method Using Free-Space Dielectrics**	
Group Art Unit **Unknown**	Confirmation Number: **Unknown**

Box Patent Application

Assistant Commissioner for Patents

Washington, D.C. 20231

Dear Sir:

Certification Under 37 C.F.R. §1.10

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Janice Pampell
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Please enter this preliminary amendment prior to examination of the Divisional Application. Please amend the Application as follows:

IN THE ABSTRACT:

Delete the existing abstract and replace it with the following.

An interconnect structure for an integrated circuit includes a free-space region to reduce RC delays between interconnects. Many different embodiments of the structure can be utilized and a few are listed. A thin conformal insulating layer can lie adjacent to the conductive material within the free space, and a thicker non-conformal insulating layer may seal openings used in creating the free space. In another embodiment, two different insulating layers can be used and have relatively high thermal conductivity. In yet another embodiment, no barrier layer is needed for metallization levels after the metallization level closest to the substrate. An optional anneal of the metallization level may be performed to improve grain size.

IN THE SPECIFICATION:

Following the title, please insert the following paragraph:

RELATED APPLICATIONS

This Application claims, under 35 U.S.C. § 120, the benefit of the filing dates of U.S. Patent Application No. 09/397,332 by inventor Mehrdad M. Moslehi entitled "Method of Fabricating an Ultra High-Speed Chip Semiconductor Integrated Circuit Interconnect Structure Using Free-Space Dielectrics" filed on September 14, 1999, and U.S. Patent Application No. 09/064,431 by inventor Mehrdad M. Moslehi entitled "Ultra High-Speed Chip Semiconductor Integrated Circuit Interconnect Structure and Fabrication Method Using Free-Space Dielectrics" filed on April 22, 1998, and hereby incorporates these applications by reference in their entireties as if they had been fully set forth herein.

On page 9, delete the paragraph starting at line 11 and replace it with the following.

Referring to Fig. 2, in damascene dielectric trench structure 22, trench 24 is filled entirely with the high conductivity metal line having electrical resistivity of ρ_m. On the other hand, damascene trench structure 20 includes barrier layer 26 (shown as a conformal layer) with a layer thickness t_b and a material resistivity of ρ_b in trench 28. The high conductivity metal line 28 occupies the remaining space surrounded by the barrier layer. Assuming $\rho_b >> \rho_m$, which is typically the case in practice, we can compare the total conductor line resistance per unit length for these two conditions:

On page 9, delete the paragraph starting at line 22 and replace it with the following.

R_1 is the conductor line resistance per unit length without the barrier layer in trench structure 22;

On page 9, delete the paragraph starting at line 24 and replace it with the following.

R_2 is the conductor line resistance per unit length with the barrier layer in trench structure 20

On page 11, delete the paragraph starting at line 6 and replace it with the following.

Similarly, the barrier layer can also degrade the effective via plug resistance. For instance, FIGURE 3 shows via plugs 30 and 32 connecting the metal lines between two adjacent interconnect levels. Via plug 30 includes a metal plug between metal lines 34 and 35 which is fully surrounded at the bottom and sidewalls by the barrier layer 36. Via plug 32, on the other hand, shows an ideal situation without a barrier layer surrounding metal plug 32 (connecting metal lines 38 and 40).

On page 11, delete the paragraph starting at line 19 and replace it with the following.

R_{p1} is the effective via plug resistance with the barrier layer of via plug 30; and

On page 11, delete the paragraph starting at line 21 and replace it with the following.

R_{p2} is the effective via plug resistance without the barrier layer of via plug 32.

On page 11, delete the paragraph starting at line 23 and replace it with the following.

Also, assume that the via plug metal has a resistivity of ρ_m (1.8 T•cm), which is preferably the same as that of the interconnect metal lines on levels N and N-1). Moreover, assume that the barrier layer is conformal, has a thickness of t_b, and a resistivity of ρ_b. Moreover, assume that $\rho_b >> \rho_m$. Let's calculate R_{p1} and R_{p2} for the two via plug structures of Fig. 3:

On page 18, delete the paragraph starting at line 10 and replace it with the following.

FIGURE 2 shows two different inlaid copper interconnect lines with and without a conductive barrier layer;

On page 18, delete the paragraph starting at line 13 and replace it with the following.

FIGURE 3 shows two different copper via plugs, one with a barrier layer, the other without a barrier layer, making electrical connections between two metal lines located on two different interconnect levels;

IN THE CLAIMS:

Please cancel Claims 2-50 without prejudice or disclaimer to the subject matter.

Please add the following new Claims:

51. (New) An interconnect structure comprising:

at least one metallization level;

a first insulating layer overlying said at least one metallization level, wherein said first insulating layer comprises a plurality of openings;

a free-space dielectric medium surrounding a portion of said at least one metallization level; and

an electrically insulating material to hermetically seal said free-space dielectric medium, wherein:

said electrically insulating material comprises a first layer and a second layer having a composition different from said first layer; and

each of said first and second layers comprises an element selected from a group consisting of nitrogen and carbon.

52. (New) The interconnect structure of Claim 51, wherein said at least one metallization level comprises:

a first metallization level; and

a second metallization level overlying said first metallization level, wherein said second metallization level does not utilize any electrically conductive diffusion barrier layer.

53. (New) The interconnect structure of Claim 52, further comprising:

a bottom electrically insulating buffer layer separating said interconnect structure from underlying transistors and isolation regions within a semiconductor integrated circuit substrate.

54. (New) The interconnect structure of Claim 53, wherein said bottom electrically insulating buffer layer comprises a diffusion barrier.

55. (New) The interconnect structure of Claim 52, wherein the free-space medium comprises a gaseous material that occupies at least a substantial fraction of regions between said first metallization level and said second metallization level.

56. (New) The interconnect structure of Claim 55, wherein said gaseous material is in a pressure range of less than 5 atmospheres.

57. (New) The interconnect structure of Claim 56, wherein said gaseous material is at or near atmospheric pressure.

58. (New) The interconnect structure of Claim 51, further comprising:

a conformal layer lying between said at least one metallization level and said free-space dielectric medium.

59. (New) The interconnect structure of Claim 58, wherein said electrically insulating material is non-conformal.

60. (New) The interconnect structure of Claim 58, wherein said conformal layer has a thickness in a range of approximately 50-200 angstroms.

61. (New) The interconnect structure of Claim 51, further comprising bonding pad openings.

62. (New) The interconnect structure of Claim 51, wherein said at least one metallization level comprises copper, silver, gold, aluminum, or a superconducting material.

63. (New) The interconnect structure of Claim 51, wherein said second layer of said electrically insulating material is selected from a group consisting of aluminum nitride, carbon, and boron nitride.

64. (New) An interconnect structure comprising:

at least one metallization level;

a first insulating layer overlying said at least one metallization level, wherein said first insulating layer includes a plurality of openings;

a free-space dielectric medium surrounding a portion of said at least one metallization level;

a conformal insulating layer lying between said at least one metallization level and said free-space dielectric medium; and

a non-conformal insulating layer that seals said openings.

65. (New) The interconnect structure of Claim 64, wherein said conformal insulating layer has a thickness in a range of approximately 50-200 angstroms.

66. (New) The interconnect structure of Claim 64, wherein:

said non-conformal insulating layer comprises a first layer, and a second layer having a composition different from said first layer; and

each of said first and second layers comprises an element selected from a group consisting of nitrogen and carbon.

67. (New) The interconnect structure of Claim 64, further comprising

a first metallization level;

a second metallization level overlying said first metallization level, wherein said second metallization level does not utilize any electrically conductive diffusion barrier layer.

68. (New) The interconnect structure of Claim 64, wherein:

said at least one metallization level comprises a first metallization level and a second metallization level; and

said free-space medium comprises a gaseous material that occupies at least a substantial fraction of regions between said first metallization level and said second metallization level.

69. (New) The interconnect structure of Claim 64, further comprising bonding pad openings.

70. (New) An interconnect structure comprising at least one metallization level, a first insulating layer overlying said at least one metallization level and including a plurality of openings, and an electrically insulating material to seal said openings, wherein said interconnect structure is formed by a process comprising:

forming said at least one metallization level,

forming a free-space dielectric medium surrounding a portion of said at least one metallization level; and

annealing said at least one metallization level to increase a grain size of at least one metal line within said at least one metallization level.

71. (New) The interconnect structure of Claim 70, wherein said annealing is performed at a temperature in a range of approximately 250-400 °C.

72. (New) The interconnect structure of Claim 70, wherein said electrically insulating material comprises:

a conformal insulating layer lying between said at least one metallization level and said free-space dielectric medium.

a non-conformal insulating layer to seal said openings.

73. (New) The interconnect structure of Claim 72, wherein said conformal insulating layer has a thickness in a range of approximately 50-200 angstroms.

74. (New) The interconnect structure of Claim 72, wherein:

said non-conformal insulating layer comprises a first layer, and a second layer having a composition different from said first layer; and

each of said first and second layers comprises an element selected from a group consisting of nitrogen and carbon.

75. (New) The interconnect structure of Claim 70 wherein the at least one metallization level comprises:

a first metallization level;

a second metallization level over said first metallization level, wherein said second metallization level does not utilize any electrically conductive diffusion barrier layer.

76. (New) The interconnect structure of Claim 70, wherein:

said at least one metallization level comprises a first metallization level and a second metallization level; and

a free-space medium comprising a gaseous material that occupies at least a substantial fraction of regions between said first metallization level and said second metallization level.

77. (New) The interconnect structure of Claim 70, further comprising bonding pad openings.

78. (New) An interconnect structure comprising:

at least one metallization level comprising:

a first metallization level; and

a second metallization level, wherein said second metallization level does not utilize any electrically conductive diffusion barrier layer;

a first insulator layer overlying said at least one metallization level, wherein said first insulator layer comprises a plurality of openings,

a free-space dielectric medium surrounding a portion of said at least one metallization level; and

an electrically insulating material to seal said openings.

79. (New) The interconnect structure of Claim 78, wherein said electrically insulating material comprises:

a conformal insulating layer lying between said at least one metallization level and said free-space dielectric medium; and

a non-conformation insulating layer to seal said openings.

80. (New) The interconnect structure of Claim 79, wherein said conformal insulating layer has a thickness in a range of approximately 50-200 angstroms.

81. (New) The interconnect structure of Claim 79, wherein:

said non-conformal insulating layer comprises a first layer, and a second layer having a composition different from said first layer; and

each of said first and second layers comprises an element selected from a group consisting of nitrogen and carbon.

82. (New) The interconnect structure of Claim 78, wherein:

at least one metallization level comprises a first metallization level and a second metallization level; and

a free-space medium comprising a gaseous material that occupies at least a substantial fraction of regions between said first metallization level and said second metallization level.

83. (New) The interconnect structure of Claim 78, further comprising bonding pad openings.

84. (New) The interconnect structure of Claim 78, wherein said second metallization level comprises an adhesion layer.

REMARKS

Applicant is amending the abstract and portions of the specification, canceling Claims 2-50 without prejudice or disclaimer, and adding Claims 51-84. Drawing changes and formal drawings are being sent in a separate paper submitted concurrently herewith. Applicant respectfully submits that the changes do not add new matter to the current Application.

Applicant respectfully requests consideration of the current Application after entry of this Preliminary Amendment, and full allowance of Claims 1 and 51-84. Applicant has made an earnest attempt to place this case in condition for allowance.

The Commissioner is hereby authorized to charge any deficiencies or credit any overpayment to Deposit Account No. 50-0456.

Respectfully submitted,

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Dated: March 6, 2002

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FIG. 1 (PRIOR ART)

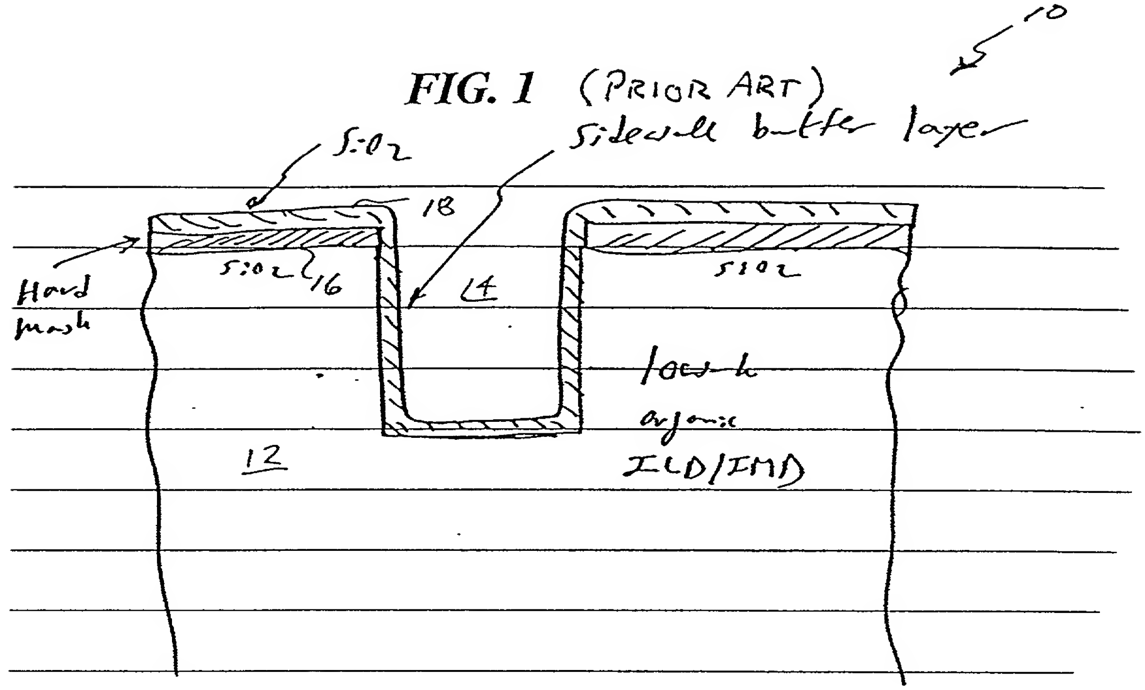
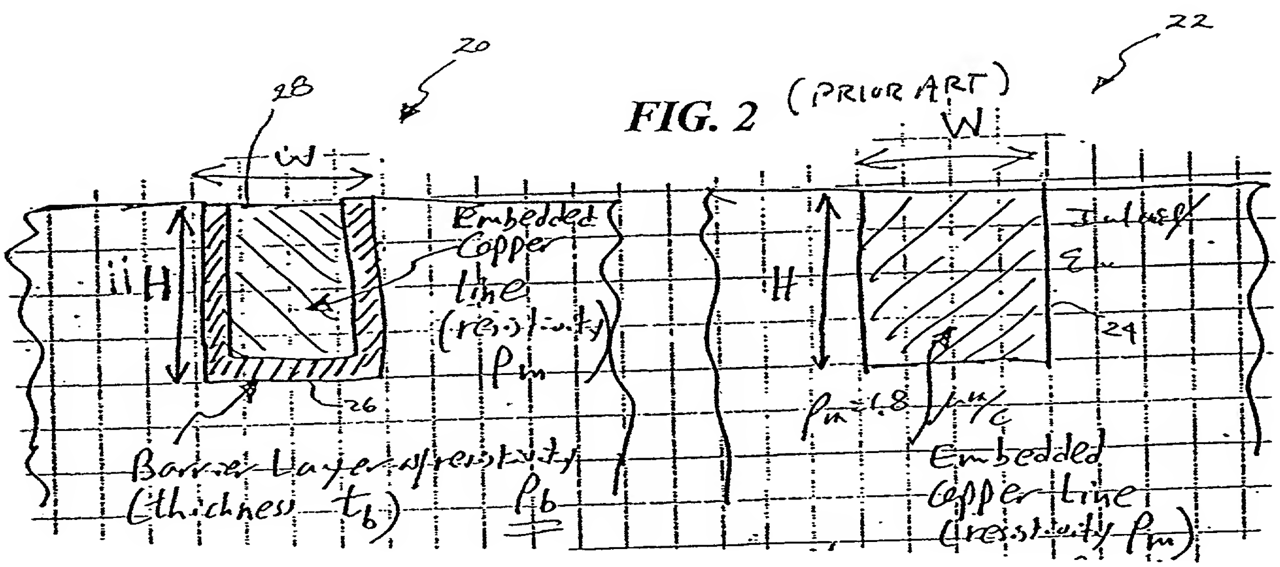


FIG. 2 (PRIOR ART)



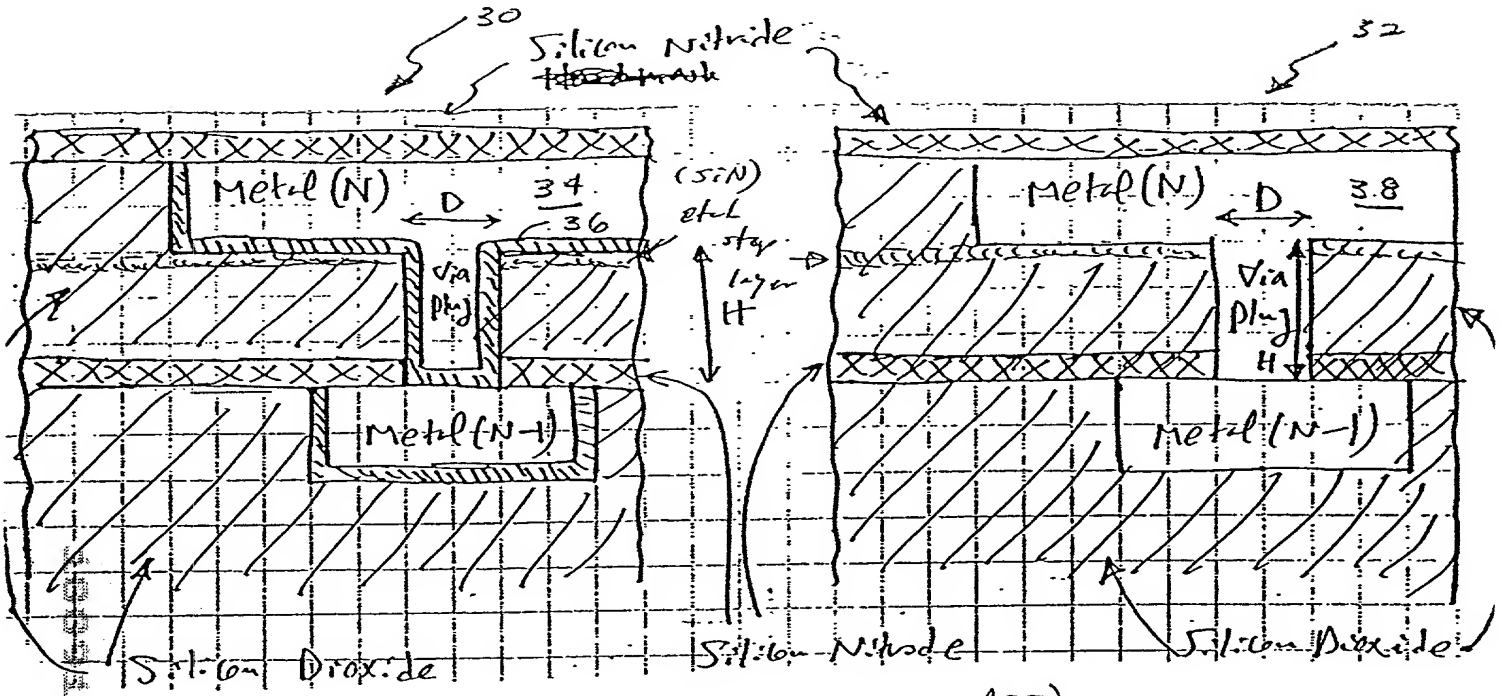


FIG. 3 (PRIOR ART)

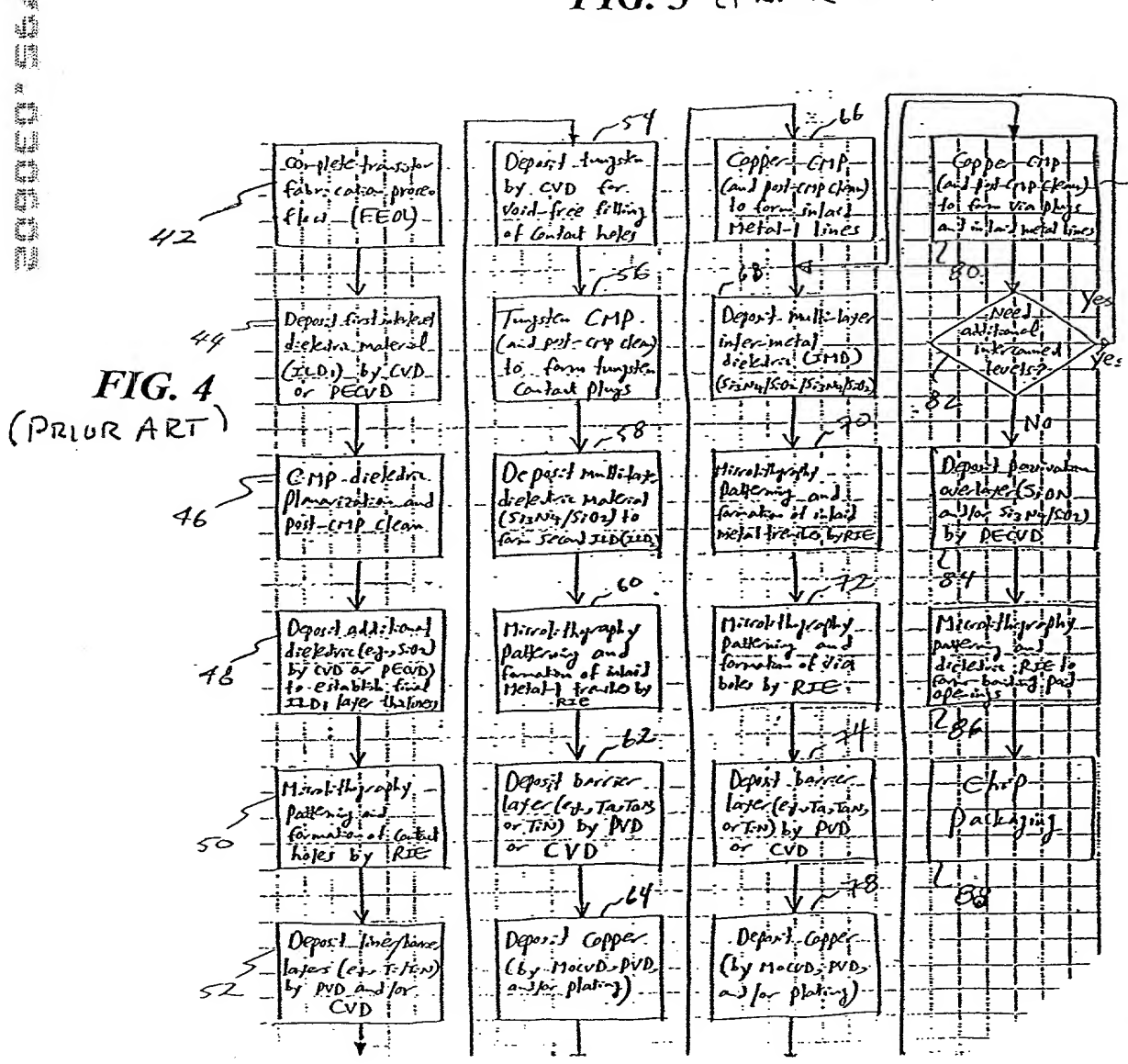


FIG. 4
(PRIOR ART)

FIG. 5 (PRIOR ART)

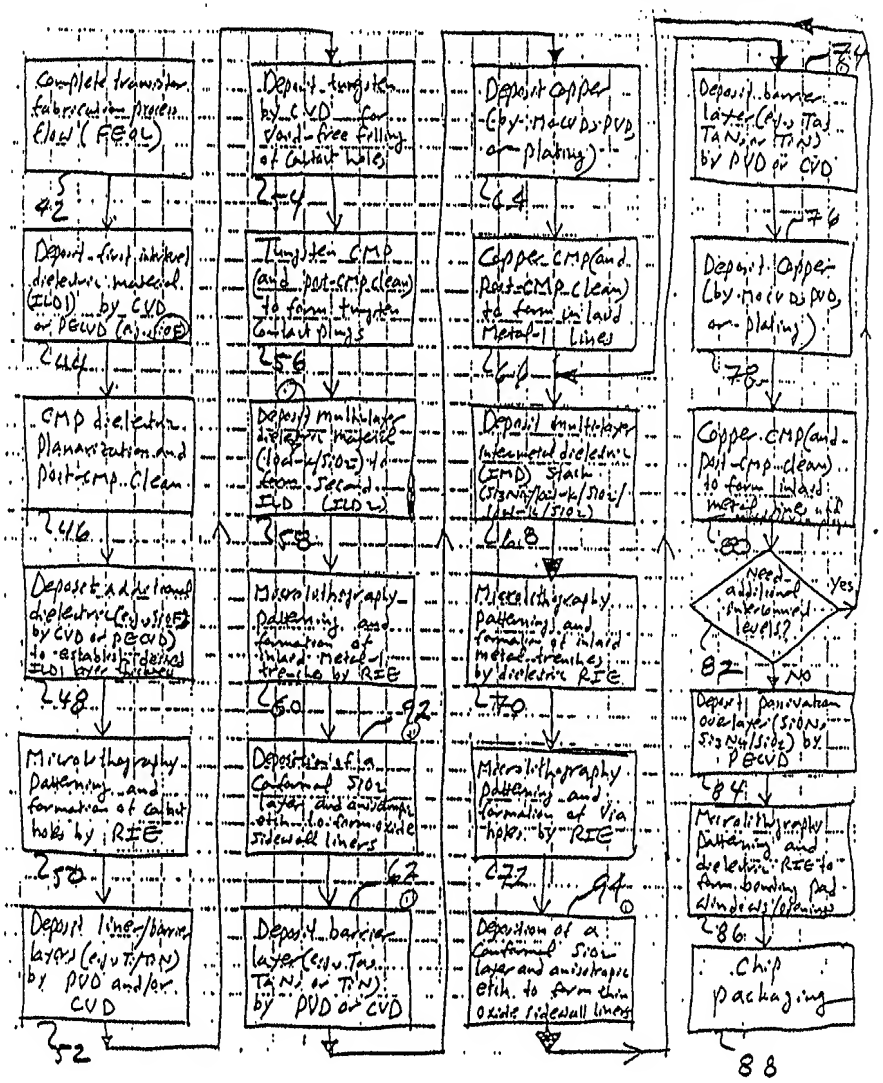


FIG. 6